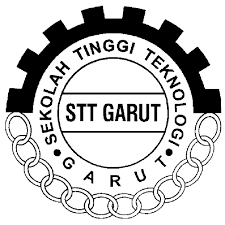
**LAPORAN PERANCANGAN SISTEM DIGITAL**

*Disusun Untuk memenuhi tugas Keamanan Sistem*



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Teknik Informatika A

**SEKOLAH TINGGI TEKNOLOGI GARUT**

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44151

ADDER

Adder 2 bit

1. Understand The Device

A= (2 bit) B=( 2bit )

Input : A= (2 bit) B=( 2bit )

Output : sum ( 3 bit )

Diagram blok

B A

Adder

2 2

AdderAdder

3

Sum

1. State The Algorithms

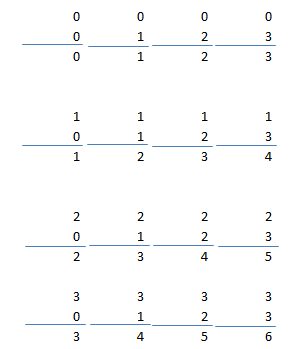
S=

A1 A0

C1 B1 B0

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_+

S2 S1 S0 1



1. Construct The Truch Table

Tabel kebenaraan Adder Desimal

|  |  |  |  |
| --- | --- | --- | --- |
| **NO** | **A** | **B** | **Sum** |
| 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 2 | 0 | 2 | 2 |
| 3 | 0 | 3 | 3 |
| 4 | 1 | 0 | 1 |
| 5 | 1 | 1 | 2 |
| 6 | 1 | 2 | 3 |
| 7 | 1 | 3 | 4 |
| 8 | 2 | 0 | 2 |
| 9 | 2 | 1 | 3 |
| 10 | 2 | 2 | 4 |
| 11 | 2 | 3 | 5 |
| 12 | 3 | 0 | 3 |
| 13 | 3 | 1 | 4 |
| 14 | 3 | 2 | 5 |
| 15 | 3 | 3 | 6 |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **A1** | **A0** | **B1** | **B0** | **S2** | **S1** | **S0** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 |

Karnaugh Map

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | B1.B0 |  |  |  |  |
| A1A0 | 00 | 01 | 11 | 10 |  |
| 00 | 0 0 | 1 1 | 1 3 | 0 2 |  |
| 01 | 1 4 | 0 5 | 0 7 | 1 6 |  |
| 11 | 1 12 | 0 13 | 0 15 | 1 14 |  |
| 10 | 0 8 | 1 9 | 1 11 | 0 10 |  |
|  |  |  |  |  | S0 |
| Cover SOP | A1 | A0 | B1 | B0 | Implikasi Primer |
| I | Ø | 1 | Ø | 0 |  |
| II | Ø | 0 | Ø | 1 | .B0 |

Fungsi :

S0 = A0 S0=A0+B0

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | B1.B0 |  |  |  |  |
| A1A0 | 00 | 01 | 11 | 10 |  |
| 00 | 0 0 | 0 1 | 1 3 | 1 2 |  |
| 01 | 0 4 | 1 5 | 0 7 | 1 6 |  |
| 11 | 1 12 | 0 13 | 1 15 | 0 14 |  |
| 10 | 1 8 | 1 9 | 0 11 | 0 10 |  |
|  |  |  |  |  | S1 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Cover SOP** | **A1** | **A0** | **B1** | **B0** | **Implikasi Primer** |
| I | 0 | 0 | 1 | Ø | ..B1 |
| II | 0 | Ø | 1 | 0 | .B1. |
| III | 1 | Ø | 0 | 0 | A1..B0 |
| IV | 1 | 0 | 0 | Ø | A1.. |
| V | 0 | 1 | 0 | 1 | .A0.B1. |
| VI | 1 | 1 | 1 | 1 | A1.A0.B1.B0 |

Fungsi :

S1 = ..B1+.B1.+A1..B0+A1..B1+.A0.B1.+A1.A0.B1.B0

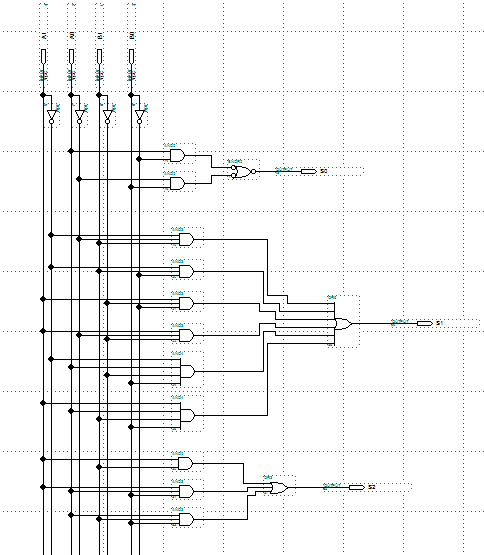
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | B1B0 |  |  |  |  |
| A1A0 | 00 | 01 | 11 | 10 |  |
| 00 | 0 0 | 0 1 | 0 3 | 0 2 |  |
| 01 | 0 4 | '0 5 | 1 7 | 0 6 |  |
| 11 | 0 12 | 1 13 | 1 15 | 1 14 |  |
| 10 | 0 8 | 0 9 | 1 11 | 1 10 |  |
|  |  |  |  |  | S2 |

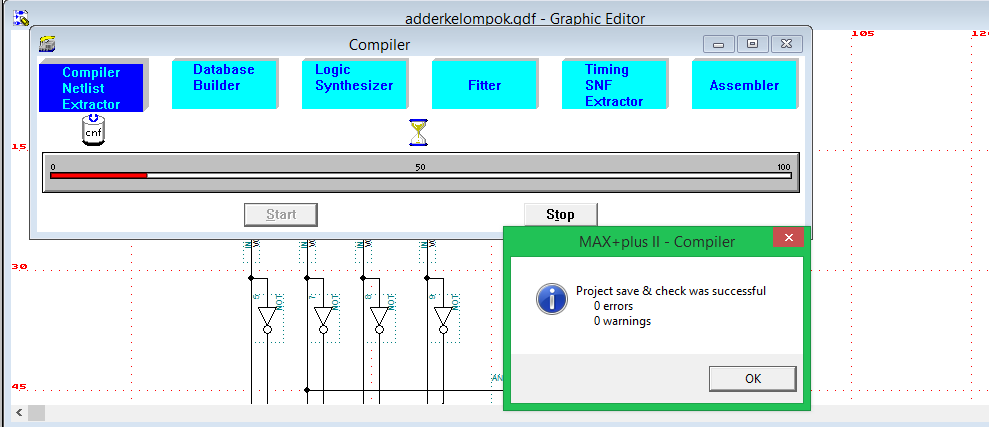
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Cover SOP** | **A1** | **A0** | **B1** | **B0** | **Implikasi Primer** |
| I | 1 | Ø | 1 | Ø | A1.B1 |
| II | 1 | 1 | Ø | 1 | A1.A0.B0 |
| III | Ø | 1 | 1 | 1 | A0.B1.B0 |

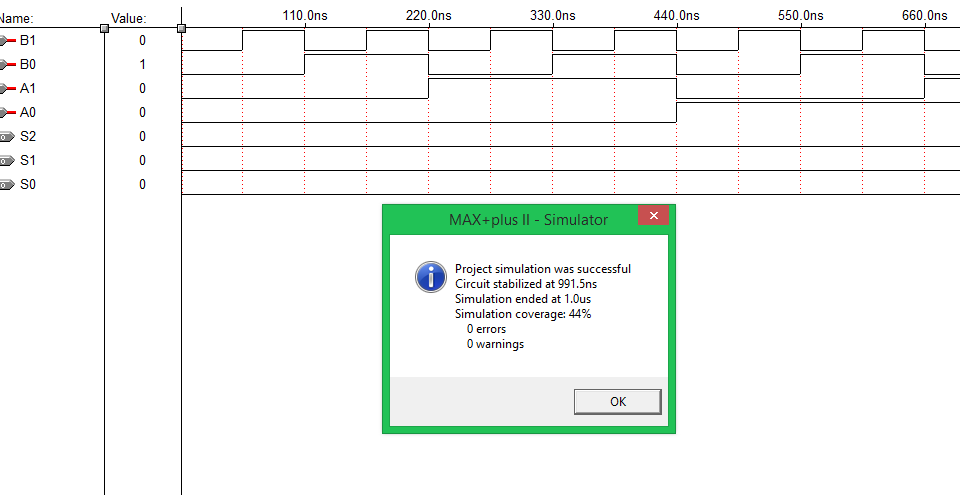
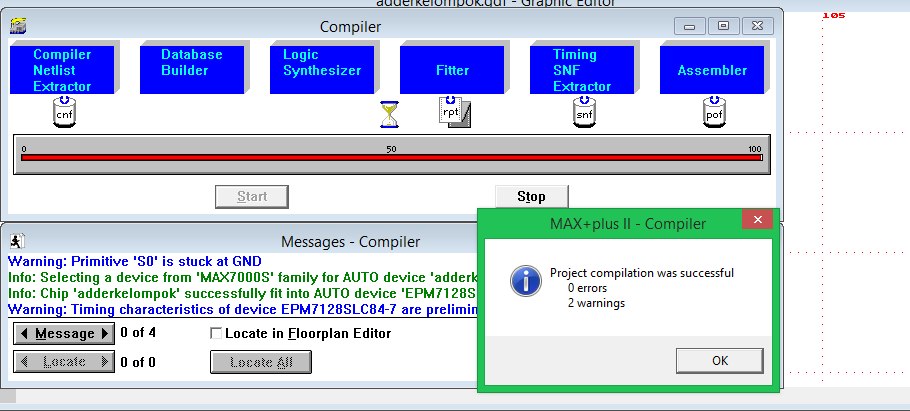
Fungsi :

S3 = A1.B1+A1.A0.B0+A0.B1.B0

Rangkaian digital







**MULTIPLIER (PENGALI)**

1. **Understand the Device**

Input : A (2 bit), B (2 bit)

2 bit : 00,01,10,11 [P max = A max X B max]

Desimal : 0,1,2,3 [P max = 3X3=9d (10012  4 bit]

Output : P = (4 bit)

Diagram Block

Multiplier

2X2

1. **State The Algorithm**

A1 A0

B1 B0 x

C0 A1B0 A0 B0

C1 A1B1 A0B1 +

P3 P2 P1 P0

1. 1 0 0 1 0 0 1
2. 1 x 0 0 x 1 1 x 1 1 x

1 1 1 0 0 1 0 0 1

1 1 + 0 0 + 1 0 + 0 1 +

1 0 0 1 0 0 0 1 1 0 0 1 1

1 1 1 1

0 1 x 1 0 x

1 1 0 0

0 0 + 1 1 +

0 1 1 1 1 0

1. **Construct The Truth Table**

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **No.** | **A** | **B** | **P=AxB** | **A1** | **A0** | **B1** | **B0** | **P3** | **P2** | **P1** | **P0** |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **1** | **0** | **1** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** |
| **2** | **0** | **2** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** |
| **3** | **0** | **3** | **0** | **0** | **0** | **1** | **1** | **0** | **0** | **0** | **0** |
| **4** | **1** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** |
| **5** | **1** | **1** | **1** | **0** | **1** | **0** | **1** | **0** | **0** | **0** | **1** |
| **6** | **1** | **2** | **2** | **0** | **1** | **1** | **0** | **0** | **0** | **1** | **0** |
| **7** | **1** | **3** | **3** | **0** | **1** | **1** | **1** | **0** | **0** | **1** | **1** |
| **8** | **2** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **9** | **2** | **1** | **2** | **1** | **0** | **0** | **1** | **0** | **0** | **1** | **0** |
| **10** | **2** | **2** | **4** | **1** | **0** | **1** | **0** | **0** | **1** | **0** | **0** |
| **11** | **2** | **3** | **6** | **1** | **0** | **1** | **1** | **0** | **1** | **1** | **0** |
| **12** | **3** | **0** | **6** | **1** | **1** | **0** | **0** | **0** | **0** | **0** | **0** |
| **13** | **3** | **1** | **3** | **1** | **1** | **0** | **1** | **0** | **0** | **1** | **1** |
| **14** | **3** | **2** | **6** | **1** | **1** | **1** | **0** | **0** | **1** | **1** | **0** |
| **15** | **3** | **3** | **9** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **1** |

**K- MAP MULTIPLIER**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | B1B0 |  |  |  |  |
| A1A0 | 0 0 | 0 1 | 1 1 | 1 0 |  |
| 0 0 | 0 | 0 | 0 | 0 |  |
| 0 1 | 0 | **1** | **1** | 0 |  |
| 1 1 | 0 | **1** | **1** | 0 |  |
| 1 0 | 0 | 0 | 0 | 0 |  |
|  |  |  |  |  | P0=A0.B0 |
|  |  |  |  |  |  |
|  |  |  |  |  |  |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Cover SOP | A1 | A0 | B1 | B0 | Implikan Primer |
| I | ∞ | 1 | ∞ | 1 | A0.B0 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | B1B0 |  |  |  |  |
| A1A0 | 0 0 | 0 1 | 1 1 | 1 0 |  |
| 0 0 | 0 | 0 | 0 | 0 |  |
| 0 1 | 0 | 0 | **1** | **1** |  |
| 1 1 | 0 | **1** | 0 | **1** |  |
| 1 0 | 0 | **1** | **1** | 0 |  |
|  |  |  |  |  | P1 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Cover SOP | A1 | A0 | B1 | B0 | Implikan Primer |
| I | 0 | 1 | 1 | ∞ | A1 A0 B1 |
| II | ∞ | 1 | 1 | 0 | A0 B1 B0 |
| II | 1 | 0 | ∞ | 1 | A1 A0 B0 |
| IV | 1 | ∞ | 0 | 1 | A1 B1 B0 |

P1= A1 A0 B1 +A0 B1 B0 +A1 A0 B0 +A1 B1 B0

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | B1B0 |  |  |  |  |
| A1A0 | 0 0 | 0 1 | 1 1 | 1 0 |  |
| 0 0 | 0 | 0 | 0 | 0 |  |
| 0 1 | 0 | 0 | 0 | 0 |  |
| 1 1 | 0 | 0 | 0 | **1** |  |
| 1 0 | 0 | 0 | **1** | **1** |  |
|  |  |  |  |  | P2 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Cover SOP | A1 | A0 | B1 | B0 | Implikan Primer |
| I | 1 | ∞ | 1 | 0 | A1 B1 B0 |
| II | 1 | 0 | 1 | ∞ | A1 A0 B1 |

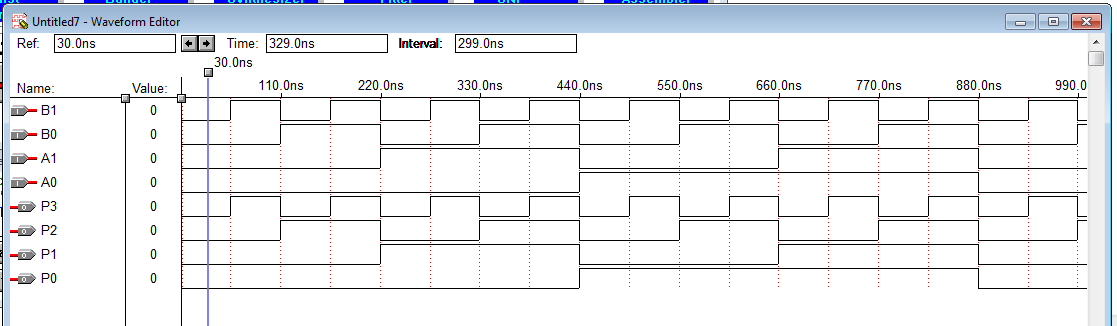
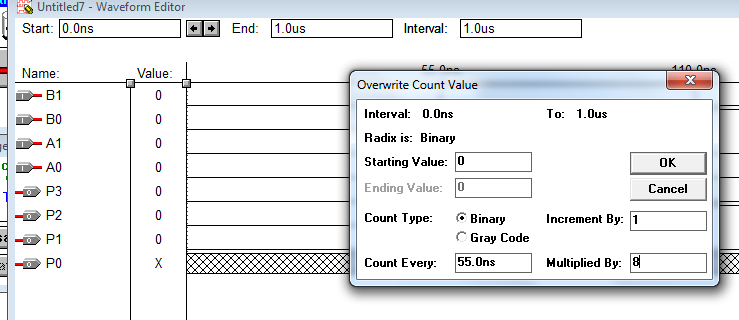
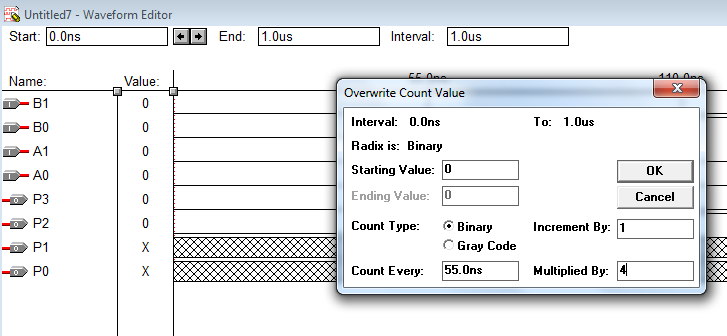
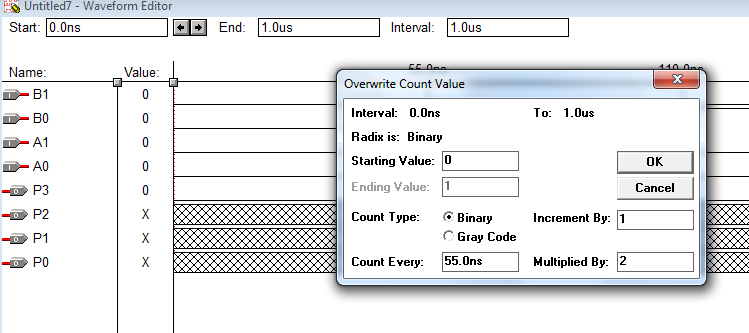
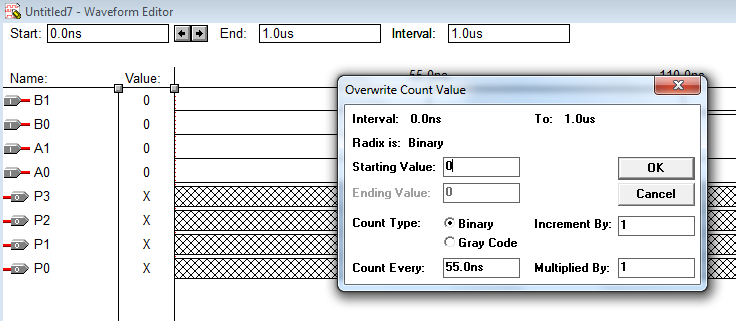
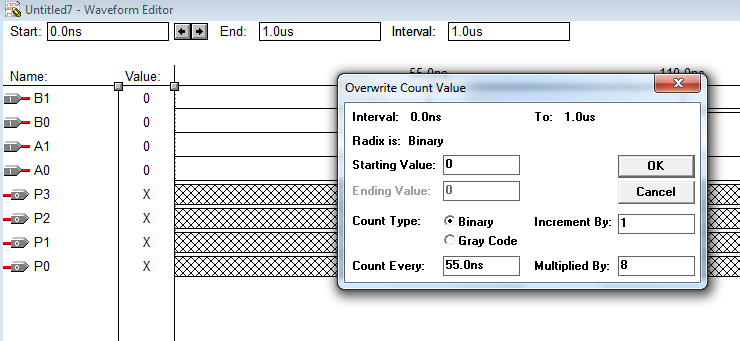
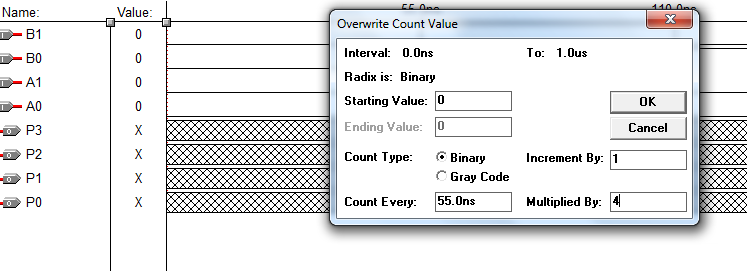
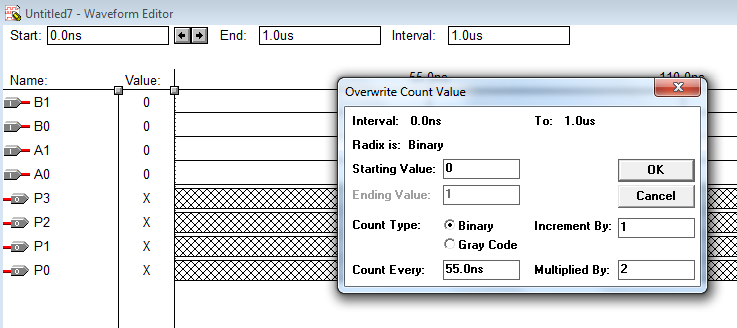
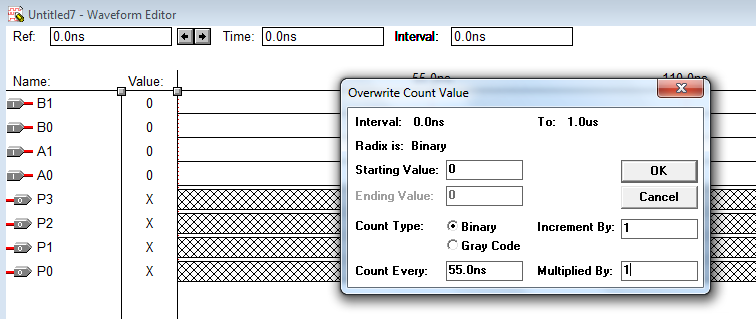
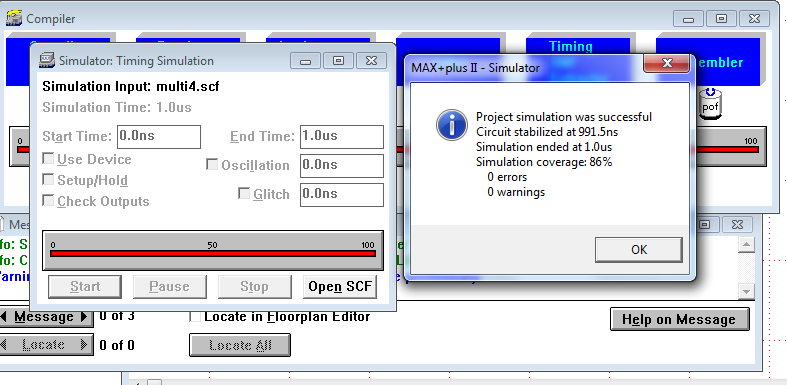
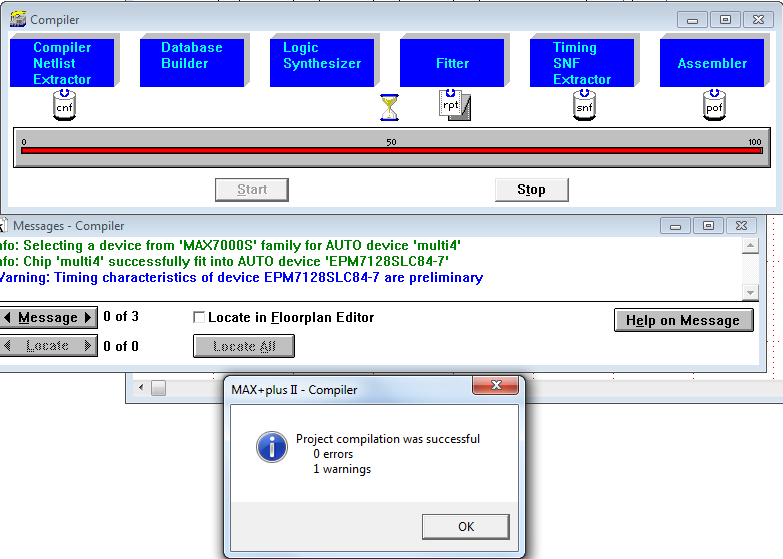
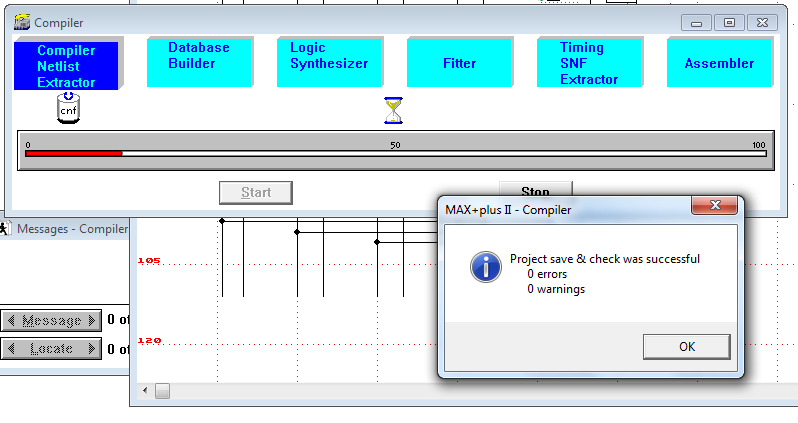
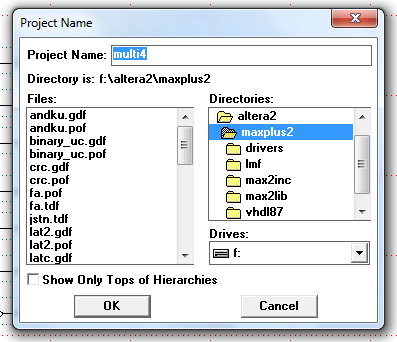
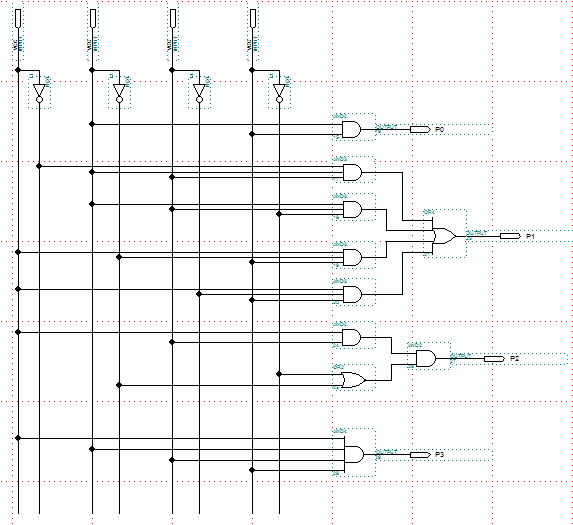
P2 = A1 B1 B0 + A1 A0 B1 = A1 B1 (B0 +A0

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | B1B0 |  |  |  |  |
| A1A0 | 0 0 | 0 1 | 1 1 | 1 0 |  |
| 0 0 | 0 | 0 | 0 | 0 |  |
| 0 1 | 0 | 0 | 0 | 0 |  |
| 1 1 | 0 | 0 | **1** | 0 |  |
| 1 0 | 0 | 0 | 0 | 0 |  |
|  |  |  |  |  | P3 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Cover SOP | A1 | A0 | B1 | B0 | Implikan Primer |
| I | 1 | 1 | 1 | 1 | A1 A0 B1 B0 |

P3= A1 A0 B1 B0

1. **SCEENSHOOT ALTERA2**

****

**SUBSTRACTER**

1. **Understand the device**

Input : A(2 bit),B(2 bit)

Output : A-B = R

R=A-B

R=3 bit

B A

Substracter

2 2

Sign R

1. **State The Algoritm**

Desimal:

|  |  |
| --- | --- |
| 0 – 0 = 0  0 – 1 = -1  0 – 2 = -2  0 – 3 = -3 | 2 – 0 = 2  2 – 1 = 1  2 – 2 = 0  2 - 3 = -1 |
| 1 – 0 = 1  1 – 1 = 0  1 – 2 = -1  1 – 3 = -2 | 3 – 0 = 3  3 - 1 = 2  3 - 2 = 1  3 – 3 = 0 |

1. **Construct The Truth Table**

Tabel Kebenaran Desimal

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| No | A | B | Sign | Reminder |
| 0 | 0 | 0 | + | 0 |
| 1 | 0 | 1 | - | 1 |
| 2 | 0 | 2 | - | 2 |
| 3 | 0 | 3 | - | 3 |
| 4 | 1 | 0 | + | 1 |
| 5 | 1 | 1 | + | 0 |
| 6 | 1 | 2 | - | 1 |
| 7 | 1 | 3 | - | 2 |
| 8 | 2 | 0 | + | 2 |
| 9 | 2 | 1 | + | 1 |
| 10 | 2 | 2 | + | 0 |
| 11 | 2 | 3 | - | 1 |
| 12 | 3 | 0 | + | 3 |
| 13 | 3 | 1 | + | 2 |
| 14 | 3 | 2 | + | 1 |
| 15 | 3 | 3 | + | 0 |

Tabel Kebenaran biner

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| No | A1 | A0 | B1 | B0 | Sign | R1 | R0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 5 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 6 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 7 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 8 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 9 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 10 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 11 | 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| 12 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 13 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 14 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 15 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |

* **K-MAP**
* **R0**

A1,A0

B1,BO

00 01 11 10

|  |  |  |  |
| --- | --- | --- | --- |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 |

00

01

11

10

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Cover Sop | A1 | A0 | B1 | B0 | Implikan Primer |
| I | Ø | 1 | Ø | 0 | A0. |
| II | Ø | 0 | Ø | 1 | .B0 |

Fungsi : R0= A0. + .B0

R0 = A0Bo

* **R1**

A1,A0

B1,BO

00 01 11 10

|  |  |  |  |
| --- | --- | --- | --- |
| 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 |

00

01

11

10

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Cover Sop | A1 | A0 | B1 | B0 | Implikan Primer |
| I | 0 | 0 | 1 | Ø | ..B1 |
| II | 0 | Ø | 1 | 1 | .B1.B0 |
| III | 1 | 1 | 0 | Ø | A1.A0. |
| IV | 1 | Ø | 0 | 0 | A1.. |

Fungsi : R1 = ..B1+ .B1.B0 + A1.A0. + A1..

R1 = ..B1+.B1.B0 )+ A1(.A0. + . )

* **Sign**

A1,A0

B1,BO

00 01 11 10

|  |  |  |  |
| --- | --- | --- | --- |
| 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |

00

01

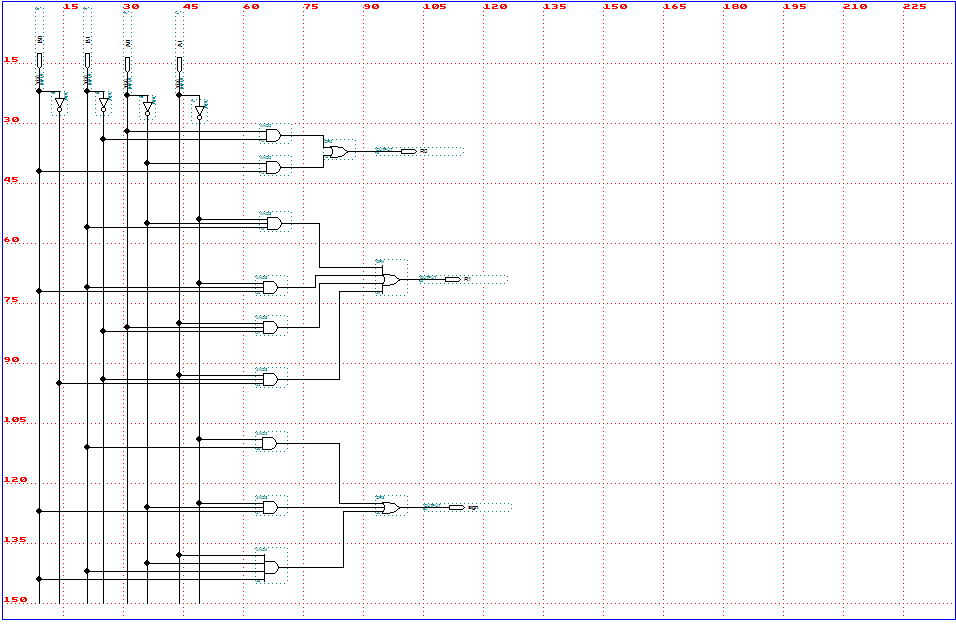
11

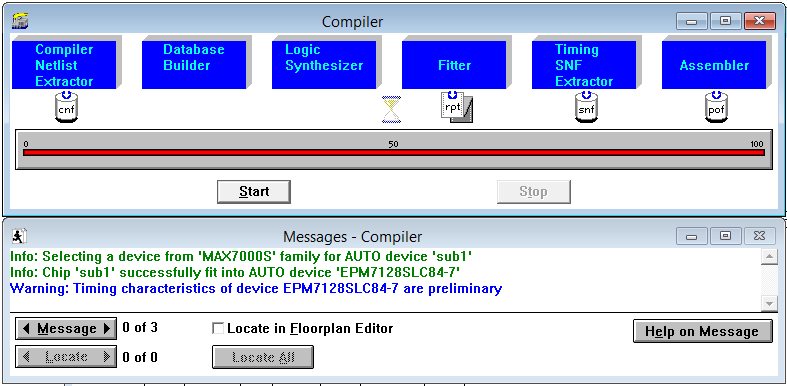
10

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Cover Sop | A1 | A0 | B1 | B0 | Implikan Primer |
| I | 0 | Ø | 1 | Ø | .B1 |
| II | 0 | 0 | Ø | 1 | .B0+ |
| III | 1 | 0 | 1 | 1 | A1..B1.B0 |

Fungsi : sign : .B1+ .B0+ A1..B1.B0

1. **Construct The Logic Diagram**





**DIVIDER**

1. **Understand The Device**

Input : A ( 2 bit ), B ( 2 bit )

Output : Hb ( 2 bit ), Sh ( 2 bit )

* Diagram Blok

A B

2 2

**DIVIDER**

2 2

Hb Sh

1. **State The Algorithms**

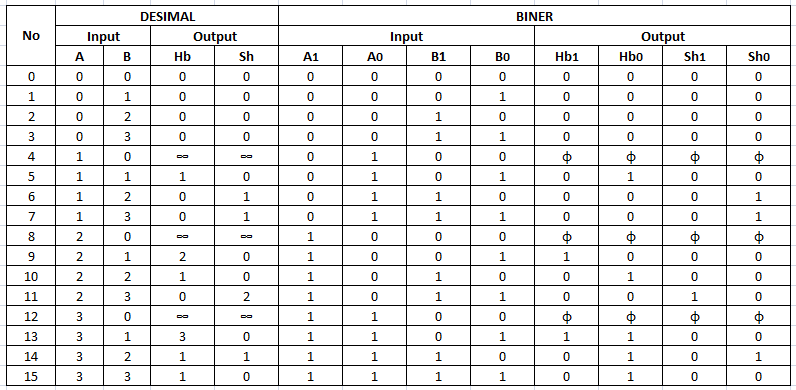
**A**

**B**

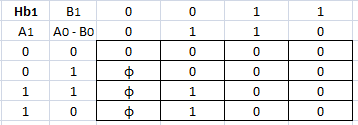
**:**

**Sh Hb**

1. **Construct The Truth Table**

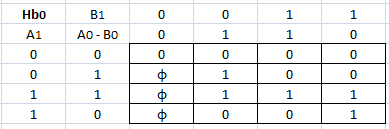


1. **Obtain The Output Functions**
2. **Hb1**



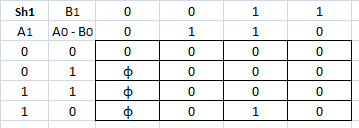
*Hb1 = A1 B1*

1. **Hb0**



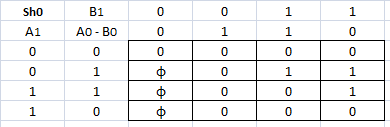
*Hb0 = A0 B1 + A1 A0 + A1 B0*

1. **Sh1**



*Sh1 = A1 A0 B1 B0*

1. **Sh0**



*Sh0 = A0 . B1 . B0 + A1 . A0 . B1*